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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/802,857
Filing Date: March 12, 2001
Appellant(s): KOH ET AL.

Ronald P. Kananen and Christopher M. Tobin
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on June 25, 2008 appealing from the Office action mailed on December 28, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, other than those identified by the appellant, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,454,100	SAGANE	9-1995
5,701,506	HOSOTANI	12-1997
5,784,537	SUZUKI et al.	7-1998
6,412,081	KOSCAL et al.	6-2002

(9) Grounds of Rejection

The following ground(s) of rejection, set forth in the Office action mailed on December 28, 2007 and incorporated herein, are applicable to the appealed claims:

- Claims 45-52 stand finally rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Appellant regards as the invention.

Claim 45

The claim recites the limitation "wherein said counter register is set to 0 during said initialization processing." There is insufficient antecedent basis for "said initialization processing" in the claim. Here, the examiner interprets the limitation as if the word "said" were omitted.

Claims 46-52

The claims are dependent upon claim 45 and are therefore indefinite for at least the same reason(s) noted above.

- Claims 27, 28 and 40 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,454,100 to Sagane ("Sagane") in view of U.S. Patent No. 5,784,537 to Suzuki et al. ("Suzuki").

Claim 27

Sagane teaches a data processing apparatus (see, for example, electronic apparatus 1 in FIG. 1) comprising:

a bug address setting register adapted to store a bug address, said bug address indicating an address for a buggy data (see, for example, interrupt generating address register 9 in FIG. 1 and column 3, lines 40-43, which shows that the register stores a correction or bug address, and column 3, lines 32-39, which shows that the correction address indicates an address for a buggy part of a program).

a coincidence detecting circuit adapted to compare said address with said bug address and output an interrupt request signal (see, for example, comparator 8 in FIG. 1 and column 3, lines 48-52, which shows that the comparator compares the execution address with the correction address and outputs a coincidence signal, and column 3, lines 59-61, which shows that the coincidence signal is output as an interrupt request signal), said interrupt request signal indicating coincidence or non-coincidence of said address and said bug address (see, for example, column 5, lines 11-16, which shows that the interrupt request signal indicates coincidence or non-coincidence of the addresses);

a central processing unit adapted to process an interrupt function upon receipt of said interrupt request signal (see, for example, CPU 2 in FIG. 1 and column 5, lines 16-21, which shows that the CPU processes an interrupt function upon receipt of the interrupt request signal).

Sagane does not expressly disclose:

a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.

Nonetheless, Sagane teaches that the interrupt request signal is generated a number of times (see, for example, steps S7 and S8 in FIG. 2). Sagane further teaches that if the ROM includes a plurality of buggy parts, then the interrupt generating address register is updated each time to reflect the next correction address (see, for example, column 5, lines 49-54). Thus, it is necessary for Sagane to track which correction address is the next correction address. To do so, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to track the number of times the interrupt request signal is generated, such as with a value stored in a register.

For example, in an analogous art, Suzuki teaches a PC comparison register section 20 that generates a ROM correction interruption request to a CPU 14 to indicate coincidence between the program address and a correction execution interruption address (see, for example, FIG. 1 and column 6, lines 27-35). Suzuki further teaches storing a value that represents the number of correcting portions (i.e., the number of buggy parts) and decrementing the value each time coincidence is indicated (see, for example, step S5 in FIG. 4A and step S28 in FIG. 4B). Thus, the value also represents the number of times coincidence is indicated.

Therefore, as Suzuki suggests, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate within the data processing apparatus of Sagane, a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.

Claim 28

The rejection of claim 27 is incorporated, and Sagane in view of Suzuki further teaches or suggests that said value is incremented when said interrupt request signal indicates said coincidence (see, for example, Suzuki, step S28 in FIG. 4B, which shows that the value is decremented when coincidence is indicated).

A person having ordinary skill in the art at the time the invention was made could, with predicable results, implement the counter register such that the value is incremented rather than decremented. Incrementing and decrementing are complementary operations. It is within the level of ordinary skill in the art to implement the teachings of Suzuki such that the value is incremented rather than decremented and achieve the intended results. For example, referring to FIGS. 4A and 4B of Suzuki, given the number of correcting portions S, one could initialize the value to 0 (rather than S) in step S5, increment (rather than decrement) the stored value in step S28, and check whether or not the stored value is equal to S (rather than 0) in step S29. Such an implementation is analogous to the one illustrated in Suzuki, and its results are predictable.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Suzuki such that said value is incremented when said interrupt request signal indicates said coincidence.

Claim 40

Sagane teaches a data processing apparatus (see, for example, electronic apparatus 1 in FIG. 1) comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes (see, for example, ROM 3 in FIG. 1 and column 1, lines 9-14, which shows that the ROM is program memory that stores instruction codes as a program, and column 3, lines 48-52, which shows that an execution or program address indicates a location in the ROM);

a bug address setting register adapted to store a bug address, said bug address indicating a starting address within said program memory for a buggy part of said program (see, for example, interrupt generating address register 9 in FIG. 1 and column 3, lines 40-43, which shows that the register stores a correction or bug address, and column 3, lines 32-39, which shows that the correction address indicates a starting address within the ROM of a buggy part of the program).

Sagane further teaches an interrupt request signal that indicates a coincidence between said program address and said bug address (see, for example, column 3, lines 59-61, which shows an interrupt request signal, and column 3, lines 48-52, which shows that the interrupt request signal indicates a coincidence between the execution address and the correction address), but does not expressly disclose:

a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address.

Nonetheless, Sagane teaches that the interrupt request signal is generated a number of times (see, for example, steps S7 and S8 in FIG. 2). Sagane further teaches that if the ROM includes a plurality of buggy parts, then the interrupt generating address register is updated each time to reflect the next correction address (see, for example, column 5, lines 49-54). Thus, it is necessary for Sagane to track which correction address is the next correction address. To do so, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to track the number of times the interrupt request signal is generated, such as with a value stored in a register.

For example, in an analogous art, Suzuki teaches a PC comparison register section 20 that generates a ROM correction interruption request to a CPU 14 to indicate coincidence between the program address and a correction execution interruption address (see, for example, FIG. 1 and column 6, lines 27-35). Suzuki further teaches storing a value that represents the number of correcting portions (i.e., the number of buggy parts) and decrementing the value each time coincidence is indicated (see, for example, step S5 in FIG. 4A and step S28 in FIG. 4B). Thus, the value also represents the number of times coincidence is indicated.

Therefore, as Suzuki suggests, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate within the data processing apparatus of Sagane, a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address.

Sagane in view of Suzuki further teaches or suggests:

wherein another program address indicates a location within said program memory for another of the instruction codes (see, for example, column 3, lines 48-52, which shows that another execution or program address indicates another location in the ROM), and

wherein said value of the counter register is incremented by 1 (see, for example, Suzuki, step S28 in FIG. 4B, which shows that the value is decremented when coincidence is indicated).

A person having ordinary skill in the art at the time the invention was made could, with predicable results, implement the counter register such that the value is incremented rather than decremented. Incrementing and decrementing are complementary operations. It is within the level of ordinary skill in the art to implement the teachings of Suzuki such that the value is incremented rather than decremented and achieve the intended results. For example, referring to FIGS. 4A and 4B of Suzuki, given the number of correcting portions S, one could initialize the value to 0 (rather than S) in step S5, increment (rather than decrement) the stored value in step S28, and check whether or not the stored value is equal to S (rather than 0) in step S29. Such an implementation is analogous to the one illustrated in Suzuki, and its results are predictable.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Suzuki such that said value of the counter register is incremented by 1.

- Claims 45-50 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over Sagane in view of U.S. Patent No. 6,412,081 to Koscal et al. ("Koscal") and in view of Suzuki.

Claim 45

Sagane teaches a data processing apparatus (see, for example, electronic apparatus 1 in FIG. 1) comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes (see, for example, ROM 3 in FIG. 1 and column 1, lines 9-14, which shows that the ROM is program memory that stores instruction codes as a program, and column 3, lines 48-52, which shows that an execution or program address indicates a location in the ROM);

a central processing unit adapted to process interrupt functions, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal (see, for example, CPU 2 in FIG. 1 and column 5, lines 16-21, which shows that the CPU processes an interrupt function upon receipt of an interrupt request signal).

Sagane does not expressly disclose that the central processing unit is adapted to process interrupt functions of different priority levels.

Nonetheless, central processing units are known to process interrupt functions of different priority levels. For example, in an analogous art, Koscal teaches processing interrupt functions to patch bugs in a program (see, for example, the abstract). Koscal further teaches that the microprocessor executes interrupt functions of different priority levels (see, for example, column 14, lines 2-7).

Therefore, as Koscal suggests, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane such that the central processing unit is adapted to process interrupt functions of different priority levels.

Sagane in view of Koscal further teaches or suggests:

a first coincidence detecting circuit adapted to compare said program address with a first bug address and output said first interrupt request signal (see, for example, comparator 8 in FIG. 1 and column 3, lines 48-52, which shows that the comparator compares the execution address with a correction or bug address and outputs a coincidence signal, and column 3, lines 59-61, which shows that the coincidence signal is output as an interrupt request signal), said central processing unit receiving said first interrupt request signal (see, for example, FIG. 1, which shows that the CPU receives the interrupt request signal via interrupt control circuit 7d);

a second coincidence detecting circuit adapted to compare said program address with a second bug address and output said second interrupt request signal (see, for example, comparator 8 in FIG. 1 and column 3, lines 48-52, which shows that the comparator compares the execution address with a correction or bug address and outputs a coincidence signal, and column 3, lines 59-61, which shows that the coincidence signal is output as an interrupt request signal), said central processing unit receiving said second interrupt request signal (see, for example, FIG. 1, which shows that the CPU receives the interrupt request signal via interrupt control circuit 7d).

Sagane teaches that if the ROM includes a plurality of buggy parts, then the interrupt generating address register is updated each time to reflect the next correction address (see, for example, column 5, lines 49-54). In an analogous embodiment, Sagane similarly teaches a correction address register that is updated to reflect the next correction address (see, for example, column 6, lines 63-67), and further suggests, as an alternative, providing a plurality of correction address registers and a plurality of comparators for the plurality of buggy parts (see, for example, column 6, line 67 to column 7, line 3). A person having ordinary skill in the art at the time the

invention was made could incorporate a plurality of comparators into the data processing apparatus of Sagane with predictable results.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane and Koscal such that it comprises first and second coincidence detecting circuits adapted to compare said program address with first and second bug addresses and output said first and second interrupt request signals, respectively.

Sagane further teaches that the interrupt request signal indicates a coincidence between said program address and said first bug address or a coincidence between said program address and said second bug address (see, for example, column 3, lines 48-52, which shows that the interrupt request signal indicates a coincidence between the execution address and the correction address), but Sagane and Koscal do not expressly disclose:

a counter register adapted to store a value, said value being incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address,

wherein said counter register is set to 0 during said initialization processing.

Nonetheless, Sagane teaches that the interrupt request signal is generated a number of times (see, for example, steps S7 and S8 in FIG. 2). As noted above, Sagane further teaches that if the ROM includes a plurality of buggy parts, then the interrupt generating address register is updated each time to reflect the next correction address (see, for example, column 5, lines 49-54). Thus, it is necessary for Sagane to track which correction address is the next correction

address. To do so, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to track the number of times the interrupt request signal is generated, such as with a value stored in a register.

For example, in an analogous art, Suzuki teaches a PC comparison register section 20 that generates a ROM correction interruption request to a CPU 14 to indicate coincidence between the program address and a correction execution interruption address (see, for example, FIG. 1 and column 6, lines 27-35). Suzuki further teaches storing a value that represents the number of correcting portions (i.e., the number of buggy parts) and decrementing the value each time coincidence is indicated (see, for example, step S5 in FIG. 4A and step S28 in FIG. 4B). Thus, the value also represents the number of times coincidence is indicated.

Therefore, as Suzuki suggests, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate within the data processing apparatus of Sagane and Koscal, a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said first bug address or a coincidence between said program address and said second bug address.

A person having ordinary skill in the art at the time the invention was made could, with predicable results, implement the counter register such that the value is incremented rather than decremented. Incrementing and decrementing are complementary operations. It is within the level of ordinary skill in the art to implement the teachings of Suzuki such that the value is incremented rather than decremented and achieve the intended results. For example, referring to FIGS. 4A and 4B of Suzuki, given the number of correcting portions S, one could initialize the

value to 0 (rather than S) in step S5, increment (rather than decrement) the stored value in step S28, and check whether or not the stored value is equal to S (rather than 0) in step S29. Such an implementation is analogous to the one illustrated in Suzuki, and its results are predictable.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane, Koscal and Suzuki such that said value is incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address, wherein said counter register is set to 0 during said initialization processing.

Claim 46

The rejection of claim 45 is incorporated, and Sagane in view of Koscal and Suzuki further teaches or suggests that said counter register is located within a random access memory at a predetermined memory address (see, for example, Suzuki, column 5, lines 41-46, which shows that the value is stored at a predetermined location in RAM).

Claim 47

The rejection of claim 45 is incorporated, and Sagane in view of Koscal and Suzuki further teaches or suggests:

bug address setting registers adapted to store said first and second bug addresses (see, for example, interrupt generating address register 9 in FIG. 1 and column 3, lines 40-43, which shows that the register stores the correction or bug address).

Claim 48

The rejection of claim 45 is incorporated, and Sagane in view of Koscal and Suzuki further teaches or suggests that said first bug address indicates a starting address within said program memory for a first buggy part of said program, and said second bug address indicates a starting address within said program memory for a second buggy part of said program (see, for example, column 3, lines 32-39, which shows that that the correction or bug addresses indicate starting addresses within the ROM of buggy parts of the program).

Claim 49

The rejection of claim 48 is incorporated, and Sagane in view of Koscal and Suzuki further teaches or suggests that said central processing unit is adapted use said value to select for correction said first buggy part or said second buggy part (see, for example, Suzuki, column 6, line 65 to column 7, line 7, which shows that the value is used to select the corresponding buggy part for correction).

Claim 50

The rejection of claim 45 is incorporated, and Sagane in view of Koscal and Suzuki further teaches that said first and second interrupt request signals are input to said central processing unit as two different interrupt request signals (see, for example, column 5, lines 49-54, which shows that the interrupt request signal is generated separately for each buggy part of the program).

- Claims 51 and 52 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over Sagane in view of Koscal and in view of Suzuki, as applied to claim 45 above, and further in view of U.S. Patent No. 5,701,506 to Hosotani ("Hosotani").

Claim 51

The rejection of claim 45 is incorporated. Sagane, Koscal and Suzuki do not expressly disclose that said first and second interrupt request signals are input to said central processing unit as a single interruption.

However, in an analogous art, Hosotani teaches a plurality of coincidence detecting circuits that each output a signal indicating a coincidence between a program address and a bug address (see, for example, match circuits 9 in FIG. 2 and column 4, lines 30-59). Hosotani further teaches that the coincidence signals are combined into a single signal (see, for example, column 4, line 60 to column 5, line 2). The teachings of Hosotani enable, for example, correcting a plurality of bugs in a program stored in a ROM without remaking the ROM (see, for example, column 1, lines 45-50).

Therefore, as Hosotani suggests, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane, Koscal and Suzuki such that said first and second interrupt request signals are input to said central processing unit as a single interruption, so as to provide an optimized approach to correcting a plurality of bugs in a program.

Claim 52

The rejection of claim 51 is incorporated, and Sagane in view of Koscal, Suzuki and Hosotani further teaches or suggests that said first and second interrupt request signals are AND'ed together to become said single interruption.

Hosotani teaches that the coincidence signals are OR'ed together, and that the resulting output is at a "1" level when any one of the address comparisons is a match and at a "0" level when all of the comparisons are mismatches (see, for example, column 4, line 60 to column 5, line 2). In other words, Hosotani defines the coincidence detection mechanism as "active high." When the mechanism is instead defined as "active low," a person having ordinary skill in art could substitute the OR gate 14 with an AND gate to achieve the same result. The resulting output from the AND gate, in this case, would be at a "0" level when any one of the address comparisons is a match and at a "1" level when all of the comparisons are mismatches.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the data processing apparatus of Sagane, Koscal, Suzuki and Hosotani such that said first and second interrupt request signals are AND'ed together to become said single interruption.

(10) Response to Arguments

"Claims 27-28 stand or fall together" (brief, pages 8-9)

Appellant's general assertion that Sagane and Suzuki "fail to disclose, teach, or suggest a bug address setting register adapted to store a bug address, said bug address indicating an address for buggy data" (brief, page 9) is merely a conclusion without any supporting analysis. As set forth in the Office action, Sagane illustrates an interrupt generating address register 9 in FIG. 1. The register stores a correction or bug address (see, for example, column 3, lines 40-43) that indicates a starting address for a buggy part of the program (see, for example, column 3, lines 32-39). Thus, Sagane teaches a bug address setting register adapted to store a bug address, said bug address indicating an address for buggy data.

"Claim 40 stands or falls alone" (brief, pages 9-13)

In response to Appellant's contention that Sagane "fails to disclose, teach or suggest a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address, wherein said value of the counter register is incremented by 1" (brief, page 10), the examiner notes that the rejection is based on a combination of references including Suzuki. For at least the reasons set forth in the Office action, the combined teachings of Sagane and Suzuki would have suggested the claimed subject matter to those of ordinary skill in the art.

Appellant contends that Suzuki "fails to disclose, teach, or suggest that [the] number of correcting portions is incremented by 1" (brief, page 10). Appellant states, "Instead, Suzuki merely teaches that the stored number of correcting portions S is decremented" (brief, page 10). Appellant further contends that the Office action "fails to provide any objective evidence sufficient to show that decrementing and incrementing the number of correcting portions are one in the same" (brief, page 10).

However, the examiner submits that the Office action establishes a *prima facie* case of obviousness. The Office action does not attempt to prove that incrementing and decrementing are "one in the same" as Appellant implies. Instead, the Office action reasons that incrementing and decrementing are complementary operations. Suzuki teaches storing a value that represents the number of correcting portions S (step S5 in FIG. 4A). Suzuki further teaches that during the "processing to set [the] ROM correction data for [the] next correcting portion," the stored value is decremented (step S28 in FIG. 4B). Then, the stored value is checked to determine whether or

not the number of correcting portions is equal to 0 (step S29 in FIG. 4B). Suzuki states, "If the number of correcting portions S is 0, the processing goes to step S33 since there is no residual correcting portion in the subroutine module of code No. m … [and] if the number of correcting portions S is not 0, the processing goes to step S30 since there [are] still residual correcting portions" (see column 6, line 65 to column 7, line 2).

In other words, Suzuki stores the value, decrements the stored value and checks whether or not the stored value is equal to 0 for the purpose of determining whether or not there are any correcting portions left to process. Indeed, Appellant's specification describes that "the counter register is increased by 1" for an analogous purpose, so that "the CPU 10 is able to judge the number of times of interrupt, that is, which number bug is being corrected, by the value of the counter register" (specification, page 26, lines 6-10).

A person having ordinary skill in the art could implement the teachings of Suzuki such that the stored value is incremented rather than decremented and achieve the same results. As noted above, incrementing and decrementing are complementary operations. It is within the level of ordinary skill in the art to implement the teachings of Suzuki such as described in the Office action and achieve the intended results. Specifically, given the number of correcting portions S, a person having ordinary skill in the art could implement the teachings of Suzuki so as to initialize the value to 0 (rather than S) in step S5, increment (rather than decrement) the stored value in step S28, and check whether or not the stored value is equal to S (rather than 0) in step S29. Such an implementation is analogous to the one described in the reference, and the results of such an implementation are predictable. Thus, the claimed subject matter would have been obvious to a person having ordinary skill in the art.

In response to Appellant's contention that the Office action "fails to show where within Suzuki there is taught that a specific amount by which the stored number of correcting portions S is decremented, or that the stored number of correcting portions S is decremented by 1" (brief, page 11), Suzuki does teach decrementing the stored value. As indicated above, the stored value tracks the number of correcting portions left to process. Thus, the examiner submits that the stored value is implicitly decremented by 1. Appellant fails to provide any evidence to the contrary. Moreover, the test for obviousness is not that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). The combined teachings of Sagane and Suzuki would have suggested the claimed subject matter to those of ordinary skill in the art.

Contrary to Appellant's argument that "incrementing is absent from within Suzuki" (brief, page 11), Suzuki clearly illustrates incrementing a position counter in step S88 of FIG. 12B (see column 9, lines 52-54). Suzuki's description of incrementing a counter is evidence that it is within the level of ordinary skill in the art to implement the teachings of Suzuki such as described in the Office action, namely such that the value is initialized to 0 in step S5 and incremented by 1 in step S28 rather than decremented.

Appellant argues that the analysis presented in the Office action amounts to "nothing more than an 'obvious-to-try' situation" (brief, page 12). In response, the examiner notes that "obvious to try," or choosing from a finite number of identified, predictable solutions with a reasonable expectation of success, is a rationale that may support a conclusion of obviousness.

See MPEP § 2141. A person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. See *KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, 82 USPQ2d 1385 (2007).

"Claims 45-51 stand or fall together" (brief, pages 13-14)

Appellant's general assertion that Sagane and Suzuki "fail to disclose, teach, or suggest a central processing unit adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal" (brief, page 14) is merely a conclusion without any supporting analysis. Moreover, the rejection is based on a combination of references including Koscal. Sagane teaches a CPU 2 in FIG. 1 adapted to process an interrupt function upon receipt of an interrupt request signal (see, for example, column 5, lines 16-21), and Koscal teaches processing interrupt functions of different priority levels (see, for example, column 14, lines 2-7). For at least the reasons set forth in the Office action, the combined teachings of Sagane, Koscal and Suzuki would have suggested the claimed subject matter to those of ordinary skill in the art.

Appellant's general assertion that Sagane and Suzuki "fail to disclose, teach, or suggest a counter register adapted to store a value, said value being incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address, wherein said counter register is set to 0 during said initialization processing" (brief, page 14) is merely a conclusion without any supporting analysis. As indicated above, and

with reference to FIGS. 4A and 4B of Suzuki, given the number of correcting portions S, a person having ordinary skill in the art could, with predictable results, implement the teachings of Suzuki so as to initialize the value to 0 (rather than S) in step S5, increment (rather than decrement) the stored value in step S28, and check whether or not the stored value is equal to S (rather than 0) in step S29. For at least the reasons set forth in the Office action, the combined teachings of Sagane, Koscal and Suzuki would have suggested the claimed subject matter to those of ordinary skill in the art.

"Claim 52 stands or falls alone" (brief, pages 15-17)

At the outset, the examiner notes that Appellant's arguments in support of dependent claim 52 are closely related to the arguments presented in the Request for Rehearing filed on December 29, 2006. In the Decision on Request for Rehearing mailed on June 21, 2007, the Board considered Appellant's arguments and accordingly denied the request.

Appellant contends that Hosotani "fails to disclose, teach, or suggest the signals from the first to third match circuits 9a-9c being input to CPU 1" (brief, page 16), but acknowledges that the "first to third match circuits 9a-9c are connected to a three-input OR circuit 14" (brief, page 17). Still, Appellant contends that Hosotani "fails to disclose, teach or suggest the signals from the three-input OR circuit 14 being input to CPU 1" (brief, page 17).

In response, the examiner notes that the rejection is based on a combination of references. As set forth in the Office action, Sagane teaches the CPU "receiving" the interrupt request signals such as recited in independent claim 45. Specifically, Sagane teaches CPU 2 receiving the interrupt request signals from interrupt control circuit 7d (see FIG. 1). The interrupt request

signals are "input to" CPU 2 in the same manner. However, Sagane does not explicitly disclose that the interrupt request signals are input to CPU 2 "as a single interruption" such as recited in claim 51. Consequently, Sagane does not explicitly disclose that the interrupt request signals are "AND'ed together" to become the single interruption such as recited in claim 52.

Nonetheless, Hosotani teaches output signals from match circuits 9a, 9b and 9c that are comparable to the interrupt request signals of Sagane (see column 4, lines 30-59). The output signals of the match circuits are "OR'ed together" with OR circuit 14 to become a single signal (see column 4, line 60 to column 5, line 2). In Hosotani, the single signal is "input to" CPU 1 indirectly by way of connection control means 10 (see FIG. 2). The language of Appellant's claims does not specify how the single interruption is "input to" the CPU.

Moreover, as noted above, the rejection is based on a combination of references. Sagane teaches that the interrupt request signals are "input to" CPU 2 from interrupt control circuit 7d (see FIG. 1). For at least the reasons set forth in the Office action, the combined teachings of Sagane, Koscal, Suzuki and Hosotani would have suggested the claimed subject matter to those of ordinary skill in the art.

In response to Appellant's contention that Hosotani "fails to disclose, teach or suggest a data processing apparatus wherein said first and second interrupt request signals are AND'ed together to become said single interruption" (brief, page 17), Hosotani does teach that the signals are "OR'ed together" (see FIG. 2). As set forth in the Office action, Hosotani further teaches that the output from OR circuit 14 is at a "1" level when any one of the address comparisons is a match and at a "0" level when all of the comparisons are mismatches (see column 4, line 60 to column 5, line 2). In other words, Hosotani defines the mechanism as "active high" as that term

is understood in the art. If the mechanism is instead defined as "active low," a person having ordinary skill in the art could substitute the OR gate with an AND gate to achieve the intended results. The output from the AND gate in such an implementation would be at a "0" level when any one of the address comparisons is a match and at a "1" level when all of the comparisons are mismatches. Thus, a person having ordinary skill in the art could implement the teachings of Hosotani such that the signals are "AND'ed together" with predictable results. The examiner submits that the Office action establishes a *prima facie* case of obviousness.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Examiner
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